THE AMENDMENTS

In The Claims

1. (Previously Presented) A processor readable, physical medium~~, which is physical,~~ encoding a data structure for supporting one or more packet modification operations, the data structure comprising:

a first pointer, entered in the data structure, to a sequence of ~~one or more~~ commands, executable by a processor, implementing one or more packet modification operations and stored, in packed format, with more than one command stored in a single addressable entry of the stored sequence, in a first memory area; and

a second pointer, also entered in the data structure, to a burst of ~~one or more~~ data or mask items, stored, in packed format, with more than one data or mask item stored in a single addressable entry of the stored burst, in a second memory area distinct from the first, for use by the processor in executing the one or more commands;

wherein ~~at least one~~the commands in the sequence ~~implements a packet modification operation that uses~~specify performing the one or more packet modification operations using, as operands or as masks for operands, ~~at least one of the one or more~~ the data or mask items in the burst~~to modify a packet~~.

2. (Previously Presented) The processor readable medium of claim 1 wherein the first and second memory areas are located in different memories.

3. (Previously Presented) The processor readable medium of claim 1 wherein the first and second memory areas are located in the same memory.

4. (Cancelled).

5. (Cancelled).

6. (Currently Amended) The processor readable medium of claim 1 wherein the ~~one or more~~ data or mask items comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

7. (Previously Presented) The processor readable medium of claim 1 wherein the first and second memory areas are located in a memory implemented off chip in relation to the processor.

8. (Previously Presented) The processor readable medium of claim 1 wherein the first memory area is located in a memory implemented on chip in relation to the processor.

9. (Currently Amended) The processor readable medium of claim 1 wherein the data structure comprises ~~one or more~~a plurality of pointers, each to a sequence of ~~one or more~~ commands implementing one or more packet modification operations.

10. (Currently Amended) The processor readable medium of claim 9 wherein the data structure comprises ~~one or more~~a plurality pointers, each to a burst of ~~one or more~~ data or mask items.

11. (Currently Amended) A method of performing one or more packet modification operations on a packet associated with a data structure link, the method comprising:

retrieving from a memory a data structure corresponding to the data structure link, the data structure comprising a first pointer, entered in the data structure, to a sequence of ~~one or more~~ commands, for execution by a processor, implementing one or more packet modification operations and stored, in packed format, with more than one command stored in a single addressable entry in the stored sequence, in a first memory area, and a second pointer, also entered in the data structure, to a burst of ~~one or more~~ data or mask items, stored, in packed format, with more than one data or mask item stored in a single addressable entry in the stored burst, in a second memory area distinct from the first, for use by the processor in executing the one or more commands;

retrieving from the first memory area the ~~one or more~~ commands in the sequence by using the first pointer;

retrieving from the second memory area the ~~one or more~~ data or mask items in the burst by using the second pointer; and

executing the ~~one or more~~ commands in the sequence by the processor, thereby performing one or more packet modification operations on the packet;

~~wherein at least one of the one or more commands retrieved from the first memory area implements a packet modification operation that uses at least one of~~ using, as operands or as masks for operands in the one or more packet modification operations, the ~~one or more~~ data or mask items in the burst ~~to modify the packet~~.

12. (Previously Presented) The method of claim 11 wherein a switch associates the data structure link with the packet.

13. (Previously Presented) The method of claim 12 wherein the switch associates the data structure link with the packet by inserting a data structure index corresponding to the link into a header of the packet.

14. (Previously Presented) The method of claim 11 wherein the first and second memory areas are located in different memories.

15. (Previously Presented) The method of claim 11 wherein the first and second memory areas are located in the same memory.

16. (Cancelled).

17. (Cancelled).

18. (Currently Amended) The method of claim 11 wherein the ~~one or more~~ data or mask items in the burst comprise data items and associated mask items, with a data item stored adjacent to its associated mask item.

19. (Previously Presented) The method of claim 11 wherein the first and second memory areas are located in a memory implemented off chip in relation to the processor.

20. (Previously Presented) The method of claim 11 wherein the first memory area is located in a memory implemented on chip in relation to the processor.

21. (Currently Amended) The method of claim 12 wherein the data structure comprises ~~one or more~~a plurality of pointers, each to a sequence of ~~one or more~~ commands implementing one or more packet modification operations.

22. (Currently Amended) The method of claim 12 wherein the data structure comprises ~~one or more~~a plurality of pointers, each to a burst of ~~one or more~~ data or mask items.

23. (Canceled)

24. (Currently Amended) A packet modification system comprising:

a memory storing a data structure comprising a first pointer, entered in the data structure, to a sequence of ~~one or more~~ commands implementing one or more packet modification operations and stored, in packed format, with more than one command stored in a single addressable entry in the stored sequence, in a first memory area; and a second pointer, also entered in the data structure, to a burst of ~~one or more~~ data or mask items, stored, in packed format, with more than one data or mask item stored in a single addressable entry in the stored burst, in a second memory area distinct from the first, for use in the one or more packet modification operations; and

a processor configured to retrieve and execute the ~~one or more~~ commands in the sequence pointed to by the first pointer, ~~wherein at least one of the one or more commands implements a packet modification operation that uses at least one of~~ using, as operands or masks of operands in the one or more packet modification operations, the ~~one or more~~ data or mask items in the burst ~~to modify a packet~~.

25.-27. (Canceled)

28. (Previously Presented) The system of claim 24 wherein the first and second memory areas are located in different memories.

29. (Previously Presented) The system of claim 24 wherein the first and second memory areas are located in the same memory.

30. (Currently Amended) The system of claim 24 wherein the processor comprises a pipeline processor core configured to retrieve the ~~one or more~~ commands in the sequence in a first stage, and execute the ~~one or more~~ commands in the sequence in one or more subsequent stages.